forming a well of a second type conductivity in the semiconductor;

forming a first type transistor in the well, wherein the first type transistor has a first source, a first drain, and a first gate;

forming a first contact in the well in spaced relation to the first type transistor;

forming a second contact in the well in spaced relation to the first type transistor;

coupling the first contact to a first voltage input; and

coupling the second contact to the first source.

36. (Amended) The method of claim 35, wherein forming a first contact comprises forming a first contact a first distance from the first source, wherein the first distance defines a first component of a parasitic resistance of the well; and

wherein forming a second contact comprises forming a second contact a second distance from the first source, wherein the second distance defines a second component of the parasitic resistance of the well.

37. (Amended) The method of claim 35 wherein:

forming a well comprises forming an n-type well in the semiconductor;

forming a first type transistor comprises forming a first p-type region in the well defining the first source, forming a second p-type region in the well defining the first drain and forming the first gate over the well.

38. (Amended) A method for fabricating a memory cell comprising:

providing a semiconductor;

doping the semiconductor to provide p-type conductivity;

forming a first inverter, wherein forming a first inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the p-type transistor;

forming a second inverter, wherein forming a second inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the p-type transistor; and

cross coupling the second inverter to the first inverter.

42. (Amended) A method of fabricating a memory cell comprising:

providing a substrate;

forming a first semiconductor structure within the substrate;

forming a first pull-up transistor having a first source and a first drain in the first semiconductor structure, and a first gate over the first semiconductor structure;

forming a first pull-down transistor having a second source and a second drain in the substrate, and a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure, each of the first and second contacts positioned in spaced relation to the first pull-up transistor;

coupling the first drain to the second drain;

coupling the first gate to the second gate; coupling the first source to the second contact; and

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through a parasitic resistance of the first semiconductor structure.

51. (New) The method of claim 35 wherein coupling the first source to the second contact comprises forming an interconnect layer over the semiconductor.

52. (New) The method of claim 51 wherein the interconnect layer comprises a metallization connection.

53. (New) The method of claim 35 wherein the first source is coupled to the first voltage input through a parasitic resistance of the well.

54. (New) The method of claim 36 wherein the the first source is coupled to the first voltage input through the series combination of the first and second components of the parasitic resistance of the well.

55. (New) The method of claim 36 wherein the first and second contacts are positioned in the well such that the distance from the first contact to the second contact is greater than the distance from the first contact to the first source.

56. (New) The method of claim 35, wherein the first type transistor is positioned between the first and second contacts.

57. (New) The method of claim 35 further comprising forming a plurality of first type transistors in the well, each of the first type transistors having a source coupled to the second contact.

58. (New) The method of claim 35 further comprising:

forming a second type transistor in the substrate outside of the well;

coupling the second type transistor to a second voltage input; and

coupling the semiconductor to a third voltage input proximate to the second type transistor.

59. (New) The method of claim 58 wherein the third voltage input comprises a substrate tie down contact.

60. (New) The method of claim 58 wherein the first type transistor comprises a pull up transistor, and wherein the second type transistor comprises a pull down transistor.

61. (New) The method of claim 58, further comprising:

forming a plurality of first type transistors formed in the well, each of the first type transistors having a source, a drain, and a gate, wherein the source of each first type transistor is coupled to the second contact;

forming a plurality of second type transistors in the substrate outside of the well; and,

coupling each of the plurality of second type transistors to a second voltage input.

62. The method of claim 61, wherein each of the plurality of second type transistors has a source, a drain, and a gate, wherein each gate of the plurality of second type transistors is coupled to an associated one of the plurality of first type transistors in the well, each source of the plurality of second type transistors is coupled to the drain of the associated one of the plurality of first type transistors in the well, and each drain of the plurality of second type transistors is coupled to the second voltage input.

IN THE ELECTION REQUIREMENT

In the Office Action, the Examiner required a restriction between the following different inventions:

Species a: Claims 31-34, a method of making a memory cell including a first and second inverter.

Species b: Claims 35-37, a method of making a first inverter.

Species c: Claim 38, a method of making a memory cell including forming a well for a first and a second inverter.

Species d: Claim39, a method of making a semiconductor device including calculating a desired distance.

Species e: Claim 40, a method of making a semiconductor device forming a first resistance equal to a second resistance.

Species f: Claim 41, a method of making a memory cell including forming a first and a second parasitic resistor.

Species g: Claim 42, a method of making a memory cell including forming a pull up and a pull down transistor.

Species h: Claims 43-45, a method of making a memory cell including forming a first and a second pull up and pull down transistor.

Species i: Claim 46, a method of making an SRAM device including a plurality of row and column lines.

Species j: Claim 47, a method of making a memory cell including coupling the first source to a first voltage.

Species k: Claims 48-49, a method of making a memory cell including forming first and second pull up and pull down transistors and coupling a third source to a first voltage.

Species l: Claim 50, a method of making a memory cell including forming a plurality of memory cells in rows and columns.

Responsive to the requirement, Applicants hereby provisionally elect, WITH TRAVERSE, the invention identified by the Examiner as Species b and elect claims 35-37 as well as newly added claims 51-58 for initial prosecution. Applicants traverse the present election requirement for the reasons set forth below.